CLAIMS

What is claimed is:

1. A memory system comprising:

a plurality of memory devices coupled one to another in a chain;

a memory controller coupled to the chain and configured to output a memory access command that is received by each of the memory devices in the chain and that selects a set of two or more of the memory devices to be accessed.

2. The memory system of claim 1 wherein the memory access command is a memory read command that selects a set of the memory devices to be read by the memory controller;

3. The memory system of claim 1 wherein the memory access command is a memory write command that selects a set of the memory devices to store a sequence of write data values.

4. The memory system of claim 1 wherein the set of memory devices comprises fewer than all the memory devices in the chain.

5. The memory system of claim 1 wherein each of the memory devices in the chain, except a last memory device, comprises an output port coupled to an input port of another of the memory devices.

6. The memory system of claim 5 wherein a first memory device in the chain comprises an input port coupled to the memory controller to receive the access command.

7. The memory system of claim 6 wherein the memory controller is coupled to the input port

of the first memory device in the chain via a point-to-point signaling path.

8. The memory system of claim 7 wherein the output port of each memory device in the chain, except the last memory device, is coupled to the input port of one other of the memory devices via a point-to-point signaling path.

9. The memory system of claim 5 wherein the last memory device comprises an output port coupled to an input port of the memory controller.

10. The memory system of claim 1 wherein each of the memory devices in the chain comprises an interface register having a buffer input and a buffer output, the buffer output of each of the memory devices, except a last memory device in the chain, being coupled to the buffer input of one other memory device in the chain via a respective point-to-point signaling path.

11. The memory system of claim 10 wherein each of the memory devices in the chain comprises a clock signal receiver coupled to receive a clock signal and having an output coupled to a strobe input of the interface register.

12. The memory system of claim 11 wherein the interface register within each of the memory devices is configured to store a value present at the buffer input in synchronism with each rising edge transition of the clock signal.

13. The memory system of claim 12 wherein the interface register within each of the memory devices is further configured to store a value present at the buffer input in synchronism with each falling edge transition of the clock signal.

14. The memory system of claim 11 wherein the interface register within each of the memory devices is configured to store a value present at the buffer input in synchronism with each falling edge transition of the clock signal.

15. The memory system of claim 11 wherein each of the memory devices further comprises a clock output driver having an input coupled to an output of the clock receiver and output coupled to an input of the clock signal receiver within another one of the memory devices.

16. The memory system of claim 10 wherein the interface register comprises a first plurality of edge-triggered storage elements each having a strobe input coupled to receive a clock signal.

17. The memory system of claim 16 wherein the interface register further comprises a second plurality of edge-triggered storage elements each having a strobe input coupled to receive a complement of the clock signal.

18. The memory system of claim 14 wherein each of the memory devices in the chain further comprises an output data buffer and a select circuit, the select circuit having a first input port coupled to the output data buffer, a second input port coupled to the interface register and, in each of the memory devices in the chain except the last memory device, an output port coupled to the buffer input of the interface register of the one other memory device.

19. The memory system of claim 1 wherein each of the plurality of memory devices is a discrete integrated circuit device.

20. The memory system of claim 1 further comprising a substrate and wherein at least a portion of the memory devices are mounted to the substrate.

21. The memory system of claim 20 further comprising sets of conductive traces formed on the substrate and coupled between respective pairs of the memory devices mounted on the substrate.

22. The memory system of claim 1 further comprising a substrate having first and second surfaces, and wherein a first portion of the memory devices are mounted on the first surface of the substrate, and a second portion of the memory devices are mounted on the second surface of the substrate.

23. The memory system of claim 22 further comprising:
a first sets of conductive traces coupled between respective pairs of the memory devices mounted on the first surface of the substrate; and
a second sets of conductive traces coupled between respective pairs of the memory devices mounted on the second surface of the substrate.

24. The memory system of claim 23 further comprising a set of conductive traces extending from one of the memory devices mounted on the first surface to one of the memory devices mounted on the second surface.

25. The memory system of claim 22 further comprising an interconnection structure coupled to the memory controller, the substrate being removably coupled to the interconnection structure.

26. A method of operation in a memory controller, the method comprising:

receiving a memory access request that specifies a range of memory addresses;

outputting a memory access command to a plurality of memory devices coupled one to another in a chain, the memory access request including selection information, based on the specified range of memory addresses, that selects a set of two or more of the memory devices to be accessed.

27. The method of claim 26 wherein the memory devices in the chain are associated with respective memory identifiers, and wherein the selection information indicates at least two of the memory identifiers.

28. The method of claim 27 wherein each of the memory identifiers indicates a position, within the chain, of the associated memory device, and wherein the selection information comprises a start memory identifier and an end memory identifier that collectively select all the memory devices disposed within the chain between the memory devices associated with the start and end memory identifiers.

29. The method of claim 28 wherein the start memory identifier and end memory identifier additionally select the two memory devices associated with the start and end memory identifiers.

30. The method of claim 26 wherein the memory access request is a read request and wherein the memory access command is a read command.

31. The method of claim 30 further comprising outputting a read-data pickup command to the

plurality of memory devices after outputting the memory access command.

32. The method of claim 31 wherein outputting a read-data pickup command comprises outputting a read-data pickup command that includes the selection information that was included in the memory access command.

33. The method of claim 31 further comprising receiving read data from the set of the memory devices selected by the selection information.

34. The method of claim 31 wherein outputting a read-data pickup command after outputting the memory access command comprises delaying, after outputting the memory access command, for a predetermined number of cycles of a clock signal before outputting the read-data pickup command.

35. The method of claim 34 wherein delaying for the predetermined number of cycles of the clock signal comprises retrieving a delay value indicative of the predetermined number of cycles of the clock signal from a storage location within the memory controller.

36. The method of claim 35 wherein retrieving the delay value from the storage location comprises retrieving the delay value from one of a plurality of storage locations within the memory controller according to the set of the memory devices to be accessed.

37. The method of claim 36 further comprising reading parameter data from each of the memory devices in the chain during a configuration operation, generating the delay value based on the parameter data and storing the delay value in the one of the plurality of storage locations.

38. The method of claim 26 wherein the memory access request is a write request and wherein the memory access command is a write command.

39. The method of claim 38 further comprising:
receiving a plurality of write data values within the memory controller; and
outputting the plurality of write data values, one after another, to the plurality of memory devices.

40. The method of claim 39 wherein outputting the plurality of write data values to the plurality of memory devices comprises outputting the plurality of write data values after outputting the write command.

41. The method of claim 40 wherein outputting the write command to the plurality of memory devices comprises outputting the write command to a first memory device in the chain via a point-to-point signaling path, and wherein outputting the plurality of write data values after outputting the write command comprises outputting the plurality of write data values, one after another, to the first memory device via the point-to-point signaling path.

42. The method of claim 26 wherein outputting the memory access command to the plurality of memory devices coupled in a chain comprises outputting the memory access command to a first memory device in the chain, the first memory device being configured to receive the memory access command and retransmit the memory access command to a next-in-line memory device in the chain.

43. The method of claim 26 wherein receiving a memory access request that specifies a range

of memory address comprises receiving a memory access request that specifies a starting address and a number of storage locations to be accessed.

44. A memory device comprising:

a first interconnect structure optionally to be coupled to a reference voltage node;

a device identifier register; and

a control circuit coupled to the first interconnect structure and to the device identifier register, the control circuit being configured to record a first predetermined device identifier in the device identifier register if the first interconnect structure is coupled to the reference voltage node.

45. The memory device of claim 44 further comprising a second interconnect structure coupled to the control circuit, and wherein the control circuit is further configured to record a device identifier received via the second interconnect structure if the first interconnect structure is not coupled to the reference voltage node.

46. The memory device of claim 45 wherein the first and second interconnect structures each comprise at least one externally accessible contact of the memory device.

47. The memory device of claim 44 further comprising a second interconnect structure coupled to the control circuit, and wherein the control circuit is further configured to output a second predetermined device identifier via the second interconnect structure.

48. The memory device of claim 47 wherein the second predetermined device identifier is the first predetermined device identifier plus a predetermined increment.

49. The memory device of claim 44 further comprising a second interconnect structure coupled to the control circuit, and wherein the control circuit is further configured to output the first predetermined device identifier via the second interconnect structure.

50. A method of operation within a memory device, the method comprising:
storing a first predetermined device identifier in a storage circuit of the memory device if a configuration signal is in a first state; and
storing, in the storage circuit, a device identifier indicated by signals received at an input interface of the memory device if the configuration signal is in a second state.

51. The method of claim 50 wherein storing a device identifier indicated by signals received at the input interface of the memory device comprises generating the device identifier by incrementing a value represented by the signals received at the input interface.

52. The method of claim 50 further comprising outputting a second predetermined device identifier at an output interface of the memory device if the configuration signal is in the first state.

53. The method of claim 52 wherein the second predetermined device identifier is the first predetermined device identifier plus a predetermined increment.

54. The method of claim 50 further comprising outputting the first predetermined identifier from the memory device if the configuration signal is in the first state, and outputting the device identifier indicated by the signals received at the input interface if the configuration signal is in the second state.

55. The method of claim 50 further comprising outputting from the memory device a device identifier that is the first predetermined identifier plus an increment value if the configuration signal is in the first state, and outputting from the memory device a device identifier that is the device identifier indicated by the signals received at the input interface plus the increment value if the configuration signal is in the second state.

56. The method of claim 55 wherein the configuration signal is a single-bit signal.

57. A semiconductor memory device comprising:

a storage array;

an input/output (I/O) interface; and

a control circuit coupled to the storage array and to the I/O interface, the storage circuit being configured to retrieve data from the storage array in response to a read command received via the I/O interface and to output the data via the I/O interface in response to an output-enable command received via the I/O interface.

58. The memory device of claim 57 further comprising a device identification register to store a device identifier, and wherein the control circuit is further configured to inspect selection information included with the read command to determine whether the device identifier is indicated by device selection information associated with the read command.

59. The memory device of claim 58 wherein the device identifier is indicated by the device selection information if the device identifier falls within a range of device identifiers indicated by the device selection information.

60. The memory device of claim 58 wherein the device selection information comprises a select value that corresponds to the semiconductor memory device, and wherein the device identifier is indicated by the device selection information if the select value is in a first state.

61. The memory device of claim 60 wherein the select value is one of a plurality of bits within the device selection information.

62. The memory device of claim 57 wherein the I/O interface comprises an input interface at a first edge of the memory device and an output interface at a second edge of the memory device.

63. The memory device of claim 62 wherein the first and second edges of the semiconductor memory device are substantially parallel to one another and disposed on opposite ends of the semiconductor memory device.

64. The memory device of claim 57 further comprising a data buffer coupled to the control circuit and the I/O interface, the data buffer being configured to store the data retrieved from the storage array at least until the output-enable command is received.

65. The memory device of claim 64 wherein the data buffer comprises a shift register to store a plurality of values that constitute the data retrieved from the storage array.

66. The memory device of claim 65 wherein the control circuit is further configured to enable the plurality of values to be shifted, one after another, out of the shift register and the

semiconductor memory device in response to receipt of the output-enable command.

67. A method of operation within a semiconductor memory device, the method comprising:
retrieving data from a storage array in response to a read command;
storing the data in a data buffer; and
outputting the data from data buffer and the semiconductor memory device in response to an output-enable command.

68. The method of claim 67 further comprising receiving the read command at an input interface of the semiconductor memory device and receiving the output-enable command at the input interface a predetermined time after receiving the read command.

69. The method of claim 68 wherein the predetermined time corresponds to a data retrieval delay of the semiconductor memory device.

70. The method of claim 67 wherein retrieving the data from the storage array in response to the read command comprises retrieving the data from the storage array if a device identifier stored in a configuration circuit of the semiconductor memory device is indicated by device selection information associated with the read command.

71. The method of claim 70 wherein retrieving the data from the storage array if the device identifier is indicated by device selection information comprises determining whether the device identifier falls within a range of device identifiers indicated by the device selection information.

72. The method of claim 71 wherein the device selection information comprises a select value

that corresponds to the semiconductor memory device, and wherein retrieving the data from the storage array if the device identifier is indicated by device selection information comprises determining whether the select value is in a first state.

73. The method of claim 72 wherein the select value is one of a plurality of bits within the device selection information.

74. The method of claim 67 wherein the data retrieved from the storage array includes a plurality of values, and wherein storing the data in the data buffer comprises storing the plurality of values in a shift register.

75. The method of claim 74 wherein outputting the data from the data buffer and the semiconductor memory device in response to the output-enable command comprises shifting the plurality of values, one after another, out of the shift register and the semiconductor memory device in response to receipt of the output-enable command.

76. A memory controller comprising:

a host interface to receive a memory read request;

a memory interface; and

a control circuit coupled to the host interface and the memory interface, the control circuit being configured to output a read command via the memory interface in response to the memory read request, delay for a first time interval, then output an data-pickup command via the memory interface to enable receipt of data requested in the memory read request.

77. The memory controller of claim 76 wherein the memory read request specifies a range of

memory addresses, and wherein the first time interval is determined according to the range of memory addresses.